

CLAIMS

What is claimed is:

- 1 1. An apparatus comprising:
2 a configurable link which permits
3 a first level of access if a computer's central processing unit (CPU)
4 is in a first power management state; and
5 a second level of access if the computer's CPU is in a second power
6 management state.
- 1 2. The device of claim 1, wherein the first power management state
2 and the second power management state each comprises a set of power
3 management states.
- 1 3. The apparatus of claim 1, further comprising:
2 a first peripheral device communicatively coupled to the
3 configurable link wherein the first level of access the peripheral device is
4 capable of operating as a conventional peripheral device.
- 1 4. The apparatus of claim 1, further comprising:
2 a first peripheral device communicatively coupled to the
3 configurable link wherein the second level of access the peripheral
4 device is capable of operating as the default bus master for the computer
5 without assistance from the CPU.

1 5. The apparatus of claim 4, wherein a peripheral device coupled to
2 the configurable link causes the configurable link to operate in the
3 second level of access when the CPU is in a second power management
4 state

1 6. The apparatus of claim 1, wherein the second power management
2 state the computer's CPU is in a sleeping state.

1 7. The apparatus of claim 1, wherein the second power management
2 state includes power modes S3-S5 as defined in the Advanced
3 Configuration and Power Interface (ACPI) specification.

1 8. The apparatus of claim 1, wherein the second level of access the
2 transfer rate over the configurable link is different than in the first level
3 of access.

1 9. The apparatus of claim 1, further comprising:
2 a first peripheral device coupled to the configurable link; and
3 an input/output hub communicatively coupling the configurable
4 link and the central processing unit (CPU).

1 10. The apparatus of claim 9, wherein the first level of access, the CPU
2 manages the input/output hub to control communications to and from
3 the first peripheral device.

1 11. The apparatus of claim 9, wherein the second level of access, the
2 configurable link enables the first peripheral device to manage the

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3 input/output hub to control communications to and from the first
4 peripheral device.

1 12. The apparatus of claim 9, further comprising
2 a second peripheral device communicatively coupled to the
3 input/output hub.

1 13. The apparatus of claim 12, wherein the second level of access, the
2 first peripheral device can communicate directly with the second
3 peripheral device without assistance from the CPU.

1 14. A method comprising:
2 configuring a link to provide a first level of access to a computer's
3 resources if the computer's central processing unit (CPU) is in a first
4 power management state; and
5 configuring the link to provide a second level of access to the
6 computer's resources if the computer's CPU is in a second power
7 management state.

1 15. The method of claim 14, further comprising:
2 coupling a peripheral device to the configurable link wherein the
3 second level of access the peripheral device is capable of operating as
4 the default bus master for the computer.

1 16. The method of claim 15, wherein the first level of access the
2 peripheral is capable of operating as a conventional peripheral device.

1 17. The method of claim 14, wherein the second power management
2 state the computer's CPU is in a sleeping state.

1 18. The method of claim 14, wherein the second power management
2 state includes power modes S3-S5 as defined in the Advanced
3 Configuration and Power Interface (ACPI) specification.

1 19. The method of claim 14, wherein a peripheral device coupled to
2 the configurable link causes the configurable link to operate in the
3 second level of access when the CPU is in a second power management
4 state.

1 20. The method of claim 14, wherein configuring the link to provide a
2 second level of access also requires configuring an input/output hub to
3 which the link couples to allow the peripheral device to become the
4 default bus master.

1 21. A system, comprising:
2 a sub-system to detect the power management state of a central
3 processor;
4 a sub-system to determine whether the central processor is in a
5 first power management state or a second power management state;
6 a sub-system to allow the central processor to manage data flow
7 over an input/output hub if the central processor is in a first power
8 management state; and

9 a sub-system to configure a link coupling the input/output hub to
10 a first peripheral device to allow the first peripheral device to manage
11 data flow over the hub if the central processor is in a second power
12 management state.

1 22. The system of claim 21, further comprising:

2 a sub-system to initiate a data transfer from the first peripheral
3 device if the central processor is in the second power management state.

1 23. The system of claim 21, further comprising:

2 a sub-system to buffer data at the first peripheral device if the
3 central processor is in the second power management state.

1 24. The system of claim 21, further comprising:

2 a sub-system to allow the first peripheral device to directly access
3 and communicate with a second peripheral device without assistance
4 from the central processor.

1 25. The system of claim 21, further comprising:

2 a sub-system to delay the central processor from transitioning
3 from the second power management state to the first power
4 management state.